Research paper

Investigations on semiconductor bridge initiators with semiconductor arrester chip used to ESD protection

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Abstract

The semiconductor arrester chip was developed to protect semiconductor bridge (SCB) initiators against electrostatic discharge (ESD). The disconnected peak voltage of the semiconductor arrester chip designed is between 169 V and 220 V. While the loading voltage is higher than the disconnected peak voltage, the semiconductor arrester chip demonstrates a low resistance conduction state, and prevented the semiconductor bridge initiator from accidental ignition caused by the ESD. Experimental results indicate that the SCB initiators without semiconductor arrester chips maybe fire in case of 25 kV electrostatic voltage. The SCB initiators with semiconductor arrester chips do not fire in the same experiment. It indicates that the semiconductor arrester chips can protect SCB initiators against pin-to-case ESD.

Keywords : electrostatic discharge (ESD), protection, semiconductor.

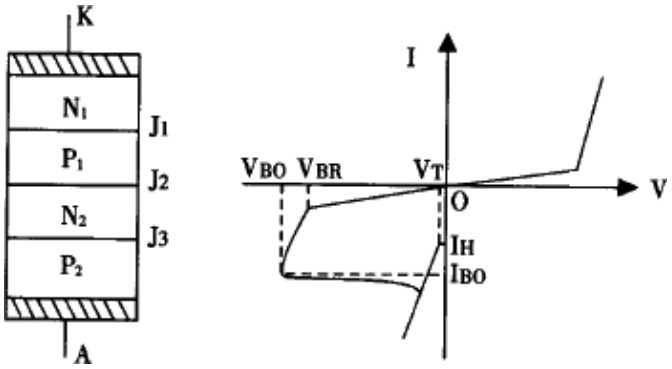
1. Introduction

The semiconductor bridge (SCB) initiator has many advantages such as low firing energy, short-function time and high-reliability[1]. However, the lack of protection for semiconductor bridges against human ESD presents an obstacle to widespread use of this device. Several techniques have been developed to protect SCB initiators or electroexplosive devices against radio-frequency interference and electrostatic discharge (ESD)[2)-7)]. M.T. Bernardo studied the surface-connectable semiconductor bridge elements and devices, in this way, doping of the polysilicon film and the side surfaces forms back-to-back diode means between opposite ones of the side surfaces. While the SCB initiators suffered pin-to-pin ESD, the diodes would provide each eventual semiconductor bridge element with unbiased protection against ESD[3]. But a major drawback of this approach is the low doping level required high breakdown voltages for a single diode and the need for different wafers (substrates) for different breakdown voltages.In order to protect the SCB initiator against pin-to-pin ESD, a parallel capacitor was used to attenuate high frequency[4)5)], and a parallel zener diode was used to limit the voltage amplitude[4]. However, this protection is lost when the diode is biased in the forword mode, therefore making the diode-protected SCB a polarized device. M.T.Bernardo investigated a voltage-protected SCB initiator element, voltage protection for SCB elements is used to prevent accidental functioning of explosive devices in the presence of stray voltage[6]. T. A. Baginski has studied the semiconductor junction EEDs insensitive to ESD and RF[7]. The goal of this research is to protect SCB initiators against pin-to-case ESD.

2. Operationan principle of semiconductor arrester chip

The semiconductor arrester chip can be regarded as a two-terminal negative resistance device which is based on the principles and structure of silicon-controlled rectifier (SCR). When the loaded voltage exceeds its avalanche voltage (or breakdown voltage), the chip can suppress the transient voltage within certain voltage. Only when the current is less than holding current, the chip resets and returns to its high impedance state. It has such characteristics like short-function time, poleless, bidirectional surge protection, high-reliability etc.

The basic structure and characteristic curve of the



(a) basic structure (b) characteristic curve

Figure 1 Diagram of the basic structure and characteristic curve of semiconductor arrester chip.

semiconductor arrester chip are shown in Figure 1.

Main parameter of semiconductor arrester chip is as follows:

V_{BR} is avalanche breakdown voltage of J_2 junction; V_{BO} is breakover voltage. Its magnitude is influenced by V_{BR} and current amplification factor α_1 of $N_1P_1N_2$; I_H is holding current. Its magnitude is influenced by breakdown voltage of J_3 junction and current amplification factor α_2 of $P_1N_2P_2$; V_T is voltage drop on conduction state.

If A is a negative voltage and K is a positive voltage, the J_1 (P_1N_1) junction and J_3 (P_2N_2) junctions are reversely biased, and J_2 (P_1N_2) junction is positively biased. For the breakdown voltage of the heavily doped J_1 junction is very low, J_3 junction bears almost all the loaded voltage. So, the volt-ampere characteristic of device is the characteristic curve of reversely biased diode. The anode current (I_A) is very small when the loaded voltage is low; the device will be broken down when the voltage is beyond breakdown voltage of junction J_3 because of the avalanche effect.

If A is a positive voltage and K is a negative voltage, the J_1 (P_1N_1) junction and J_3 (P_2N_2) junction are positively biased, while J_2 (P_1N_2) junction is reversely biased.

3. Fabrication of semiconductor arrester chip

According to the micro-electronics technology, a layer of SiO_2 is oxidized on both sides of the single-crystal silicon base. Then, the base region is selectively etched on both sides of the SiO_2 layer. In succession, the boron is diffused into the base and then the phosphor is diffused into the boron region. The depth of phosphor region is half of the boron region. The breakdown voltage of semiconductor arrester chip is designed to 200 V. The shape is square and the size is 1.5 mm×1.5 mm.

The semiconductor arrester chip is packaged on the ceramic header used in the SCB initiator. One electric pole of the arrester chip is connected to one pin of SCB and the other electric pole to the case. Therefore, it can prevent pin-to-case ESD from damaging SCB initiator. The protection principle of pin-to-case is shown in Figure 2, in which A and B represent two pins of SCB and C is the case of the SCB initiator.

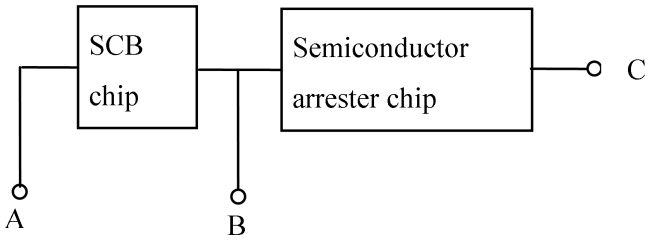


Figure 2 Pin-to-case ESD protection for SCB initiator.

Table 1 The breakdown voltage of semiconductor arrester chip.

sample number	breakdown voltage of the positive [V]	breakdown voltage of the negative [V]
1	180	169
2	210	212
3	215	220
4	172	180
5	220	220
6	218	216
7	218	218
8	214	216
9	218	220

4. Performances testing of semiconductor arrester chip

The semiconductor arrester chip is connected between the pin and the case of SCB initiator. DF4810 transistor curve tracer is used to test its performances. If the case is connected to the anode of curve tracer, it is considered as the positive. Conversely, if the case is connected to the cathode of curve tracer, it is considered as the negative. The testing results are shown in Table 1.

From the above experimental data, we may note that all the breakdown voltages of the manufactured arrester chips are between 169 V and 220 V. While using the semiconductor arrester chip to protect SCB initiator against ESD, because the electrostatic voltage is generally high, it can achieve the breakdown voltage and arrester chip will show a low-impedance conduction state. When the electrostatic pulse passes, it will return to the high-impedance state. Because the firing voltage of SCB initiators generally does not exceed 100 V, the semiconductor arrester chip will not be broken through and shows a high-impedance state. So it will not affect the normal firing of SCB.

5. The anti-electrostatic discharge research of SCB

5.1 Fabrication of SCB

The structure of SCB chip is shown in Figure 3. The SCB, is a heavily doped (~10^{20}cm^{-3}) silicon area between the aluminum lands. The aluminum lands provide a means for electric contact to the bridge. The doping element is phosphorus. The SCB can be described by its length (L), width (W), and thickness (T) to yield 1.0 Ω static resistance. L of the bridge is determined by the two aluminum lands. W is determined by the shape of the doped silicon region. T is determined by the thickness of

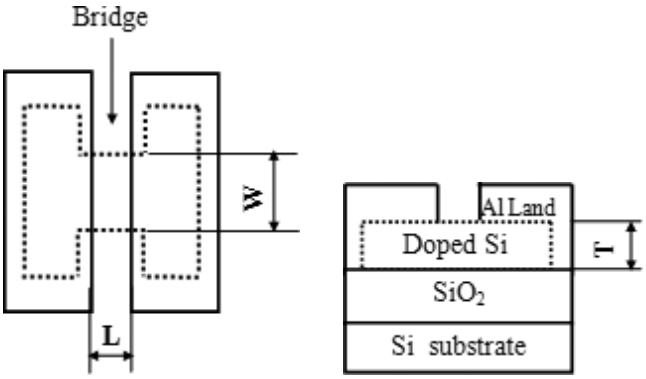


Figure 3 Simplified sketch of SCB chip.

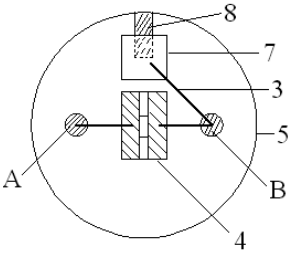


Figure 4 (a) Sketch diagram of SCB packaged semiconductor arrester chip.

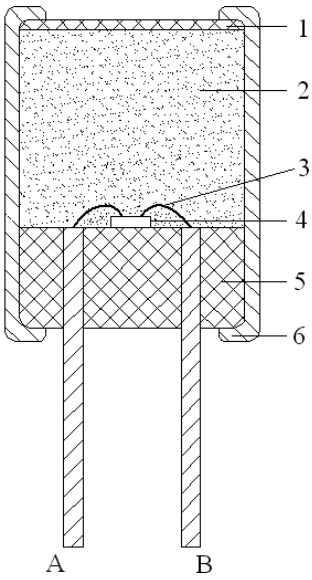


Figure 4 (b) Schematic diagram of SCB initiator.

1-cover plate 2-LTNR 3-Al wire 4-SCB chip 5-ceramic header 6-aluminum case 7-semiconductor arrester chip 8-metalization layer

the silicon layer on the silicon substrate. In this experiment, the SCB chip size is 1.4 mm×1.8 mm and the SCB dimensions is 100 μm(L)×20 μm(W)×2 μm(T) with a nominal resistance of 1.0 Ω.

The package schematic diagram of the SCB chip and the semiconductor arrester chip is shown in Figure 4. The SCB chip was bonded to the header base between the pins with a thermally conductive epoxy. Aluminum wires were thermalsonically bonded to the header pins and the aluminum lands on the SCB chip.The semiconductor arrester chip was bonded to the metal region on the header base near the SCB chip with an electrically conductive epoxy. Aluminum wires were thermalsonically bonded to the B pin and the upper electrode of the semiconductor arrester chip. The lower electrode of the semiconductor arrester chip and the aluminum case were electrically connected by the metalization layer on the ceramic header. The connecting electrical principle is shown in Figure 2.

The SCB initiator used for the experiments in this paper

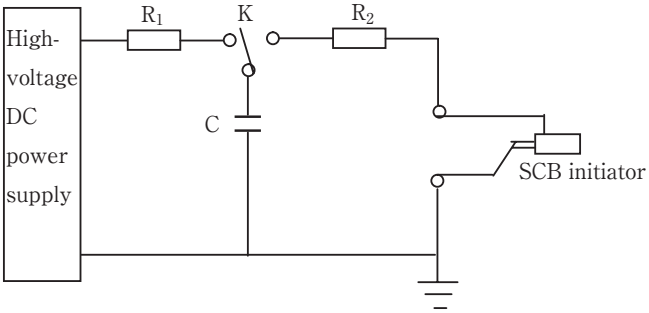


Figure 5 Schematic diagram of ESD experiment.

Table 2 The ESD experimental results of the SCB initiators.

Shot #	Protection	Electrostatic voltage [kV]	First ESD tested	Second ESD tested
1	None	25	Fire	/
2		25	No fire	No fire
3		25	No fire	No fire
4		25	No fire	No fire
5		25	No fire	No fire
6		25	No fire	Fire
7		25	No fire	Fire
8		25	No fire	No fire
9		25	No fire	No fire
10		25	No fire	No fire
11		25	No fire	No fire
12	Semiconductor	25	No fire	No fire
13	arrester chip	25	No fire	No fire
14		25	No fire	No fire
15		25	No fire	No fire
16		25	No fire	No fire

is shown in Figure 4. It consists of a ceramic header with two kovar pins, aluminum case and pyrotechnic material. The ceramic was pressed into the aluminum case. Then the devices were loaded with 30 mg of lead styphnate that was pressed against the SCB at 200 kg/cm^2.

5.2 The principle of ESD test

The schematic diagram of ESD test of SCB initiators is shown in Figure 5. For the evaluation of semiconductor arrester ESD protection behaviors to SCB initiator, the ESD experiment was performed according to GJB 5309.14 −2004 (Test method of initiating explosive device - Electrostatic sensitivity test for electric initiating explosive device). The capacitor C is 500 ± 25 pF, and the resistance of discharge resistor R2 is 5000 ± 500 Ω. In the experiment, the capacitor C was charged, and then the discharge circuit switch was closed for discharging. In this way, the electrostatic voltage was applied to SCB initiator.

5.3 Results and discussion of ESD test

The experimental results are shown in Table 2. One of the SCB initiators without semiconductor arrester chips fired in the first test. Two of the SCB initiators without semiconductor arrester chips fired in the second test. The SCB initiators with semiconductor arrester chips did not fire in the ESD tests.

As the breakdown voltage of the semiconductor arrester chip, which is between 169 V and 220 V, is much lower than the electrostatic voltage (25 kV), the chip becomes conductive sharply when suffered the pin-to-case electrostatic. Then the electrostatic energy is released through the chip. As a result, the spark produced by electrostatic breakdown is avoided between the pin and case of initiator. On the contrary, without the semiconductor arrester chip, the sparks may cause accidental ignition at 25 kV electrostatic charge. It shows that the semiconductor arrester chips can protect the SCB initiators against pin-to-case electrostatic discharge.

Conclusions

The semiconductor arrester chip is developed to protect the SCB initiator against the pin-to-case ESD in this paper. The disconnected peak voltage of semiconductor arrester chip designed is between 169 V and 220 V. As electrostatic voltage is higher than the disconnected peak voltage, the semiconductor arrester chip will transfer into the conduction state and discharges electrostatic. The SCB chip and the semiconductor arrester chip are packaged on a ceramic header. The semiconductor arrester chip is assembled between the pin and case. The electrostatic discharge tests show that the semiconductor arrester chips can protect the SCB initiators against pin-to-case ESD.

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